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ATTORNEY DOCKET NO. 10010215-1

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Inventor(s): Brian James Misek

Serial No.: 09/981,957 **Examiner:** LUU, THANH X.

Filing Date: 10/16/2001 **Group Art Unit:** 2878

Title: SEQUENTIAL READ-OUT METHOD AND SYSTEM THAT EMPLOYS A SINGLE AMPLIFIER FOR MULTIPLE COLUMNS

COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria VA 22313-1450

TRANSMITTAL OF APPEAL BRIEF

Sir:

Transmitted herewith is the Appeal Brief in this application with respect to the Notice of Appeal filed on May 20, 2006

The fee for filing this Appeal Brief is (37 CFR 1.17(c)) **$500.00.**

(complete (a) or (b) as applicable)

The proceedings herein are for a patent application and the provisions of 37 CFR 1.136(a) apply.

☐ (a) Applicant petitions for an extension of time under 37 CFR 1.136 (fees: 37 CFR 1.17(a)(1)-(5)) for the total number of months checked below:

☐	one month	$ 120.00
☐	two months	$ 450.00
☐	three months	$1020.00
☐	four months	$1590.00

☐ The extension fee has already been filled in this application.

☒ (b) Applicant believes that no extension of term is required. However, this conditional petition is being made to provide for the possibility that applicant has inadvertently overlooked the need for a petition and fee for extension of time.

Please charge to Deposit Account **50-3718** the sum of 500. At any time during the pendency of this application, please charge any fees required or credit any overpayment to Deposit Account **50-3718** pursuant to 37 CFR 1.25.

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Date of Facsimile: July 19, 2006

Typed Name: Eric Ho

Signature: Eric Ho

Respectfully submitted,

Brian James Misek

By Eric Ho

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Reg. No. 39,711

Date: July 19, 2006

Telephone No. 818-998-7220

Rev 12/05 (AplBrief)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

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Applicant	:	Brian James Misek
Filed	:	October 16, 2001
TC/A.U.	:	2878
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Commissioner For Patents
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APPEAL BRIEF (under 37 CFR 41.37 and MPEP 1205 to 1205.03)

Table of Contents:

i) REAL PARTY IN INTEREST

The real party in interest is Avago Technologies General IP (Singapore) Pte. Ltd., the assignee of record.

ii) RELATED APPEALS AND INTERFERENCES

Appellant is unaware of any prior or pending appeals, interferences or judicial proceedings, which may be related to, directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

iii) STATUS OF CLAIMS

Claims 3, 5-8, 11, 14-17, 22-30 are the subject of this appeal. Applicant appeals claims 3, 5-8, 11, 14-17, 22-30. No other claims are pending. Claims 1, 2, 4, 9, 10, 12, 13, 18-21 and 31 have been cancelled. All of the pending claims have been rejected in the Final Office Action, mailed March 20, 2006.

iv) STATUS OF AMENDMENTS

There were no amendments to the claims filed subsequent to the final rejection.

v) SUMMARY OF CLAIMED SUBJECT MATTER

One embodiment of a readout circuit according to the present invention is recited in claim 23. Specifically, claim 23 recites a readout circuit 20 that includes a first sampling circuit (see SAMPLE CIRCUIT_1 of FIG. 1) with a first electrode for coupling to a first column and a second electrode and a first switch (see COLUMN SWITCH_1 of FIG. 1). The first switch (COLUMN SWITCH_1) has a first electrode coupled to the second electrode of the first sampling circuit 24, a second electrode, and a third electrode for receiving a first sample control signal. The first switch (COLUMN SWITCH_1) selectively couples the first electrode of the first switch to the second electrode of the first switch when the first sample control signal is asserted. The first sampling circuit 24 samples a light signal and a reset signal from each photocell in the first column

The readout circuit also includes a second sampling circuit (see SAMPLE CIRCUIT_2 of FIG. 1) that includes a first electrode for coupling to a second column and a second electrode and a second switch (see COLUMN SWITCH_2 of FIG. 1) that includes a first electrode coupled to the second electrode of the second sampling circuit, a second electrode, and a third electrode for receiving a second sample control signal. The second switch (COLUMN SWITCH_2) selectively couples the first electrode of the second switch to the second electrode of the second switch when the second sample control signal is asserted. The second sampling circuit (SAMPLE CIRCUIT_2) samples a light signal and a reset signal from each photocell in the second column.

The sequential readout circuit 20 can include a single charge conversion circuit (e.g., an amplifier) 30 that includes a negative input terminal coupled to the second electrode of the first switch (COLUMN SWITCH_1) and second electrode of the second switch (COLUMN SWITCH_2). The amplifier 30 includes an output terminal for generating a signal that

corresponds to the amount of light received by a particular photocell in the array. See pages 7 to 9 of the instant specification for a detailed description of the sequential readout circuit 20 recited in claims 22 and 23. An exemplary implementation of the sequential readout circuit system is depicted in FIG. 2. FIG. 4 is a flowchart that illustrates the steps performed by the sequential readout circuit (see, e.g., pages 10 to 12 of the instant specification).

One embodiment of a system that includes the readout circuit according to the present invention is exemplified in claim 22. Claim 22 recites a system 10 that includes an array 14 of photocells and the sequential readout circuit 20. See, for example, pages 6 and 7 of the instant specification for a detailed description of the system embodied in claim 22. An embodiment of this system is also depicted in FIG. 1. The array 14 includes a plurality of photocells 18 that are typically arranged in rows and columns.

vi) GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

Whether claims 3, 5, 11, 14, and 22-30 are unpatentable under 35 U.S.C. 102(e) as being anticipated by Yonemoto et al. (US Pat. No. 6,166,769), which is hereinafter referred to as "Yonemoto" or as "the Yonemoto reference."

Whether claims 6, 7, 15, and 16 are unpatentable under 35 U.S.C. 103(a) over Yonemoto et al. (U.S. Pat. No. 6,166,769) in view of Simerly et al. (U.S. Pat. No. 5,982,424), which is hereinafter referred to as "Simerly" or as "the Simerly reference."

Whether claims 8 and 17 are unpatentable under 35 U.S.C. 103(a) over Yonemoto et al. (U.S. Pat. No. 6,166,769) in view of Krymski et al. (U.S. Pat. No. 6,222,175), which is hereinafter referred to as "Krymski" or as "the Krymski reference."

vii) ARGUMENT

Rejection under 35 U.S.C. 102(e) over Yonemoto et al. (US Pat. No. 6,166,769)

Claims 3, 5, 22, 25, 27, and 28

Claims 3, 5, 22, 25 and 27 are rejected under 35 U.S.C. 102(e) for the reasons set forth on pages 3-4 of the Action. Specifically, claims 3, 5, 22, 25 and 27 are rejected under 35 U.S.C. 102(e) as being anticipated by Yonemoto et al. (US Pat. No. 6,166,769), which is hereinafter referred to as "Yonemoto" or as "the Yonemoto reference."

The rejections under 35 U.S.C. 102(e) are respectfully traversed, and reconsideration and reexamination of the application is respectfully requested for the reasons set forth herein below.

The Federal Circuit has ruled, "Under 35 U.S.C. §102, anticipation requires that each and every element of the claimed invention be disclosed in the prior art. . . . In addition, the prior art reference must be enabling, thus placing the allegedly disclosed matter in the possession of the public." Akzo N.V. v. United States Int'l Trade Comm'n, 1 USPQ 2d 1241, 1245 (Fed. Cir. 1986), cert. denied, 482 U.S. 909 (1987). [emphasis added.]

Furthermore, the Federal Circuit has held, "Anticipation requires the disclosure in a single prior art reference of each element of the claim under consideration." W.L. Gore & Assocs. v. Garlock, Inc., 220 USPQ 303, 313 (Fed. Cir. 1983), cert. denied, 469 U.S. 851 (1984). [emphasis added.]

It is respectfully submitted that the Yonemoto reference fails to teach or suggest each and every element of the system as claimed. Specifically, the Yonemoto reference fails to teach or suggest, the first sampling circuit as claimed in claim 22. For example, the Action cites elements 38 and 38' of Yonemoto et al. taken together to teach the first sampling circuit as claimed. However, elements 38 and 38', whether alone, or in combination fail to fairly

teach or suggest the first sampling circuit, the first switch, and the specific limitations regarding the coupling between the first sampling circuit and the first switch as required by independent claim 22.

The Action dated 12/8/05 includes on page 5 a copy of FIG. 4 of the Yonemoto reference with Examiner's notations indicating how Examiner is applying Yonemoto to the claimed invention. However, combining circuit 38 and 38' to teach a first sampling circuit as claimed appears to contradict the clear teaching of Yonemoto et al. For example, Col. 7, lines 15-20 of Yonemoto et al. states, "The first operation switches 37, the first load capacitance elements 38, and the first horizontal switches 39 jointly make up a first signal holding circuit 51 for holding signals of the pixel MOS transistors before the pixels are reset." In other words, Yonemoto et al. considers elements 37, 38 and 39 to comprise a first signal holding circuit 51. Similarly, col. 7, lines 18-22 of Yonemoto et al. states, "The second operation switches 37', the second load capacitance elements 38', and the second horizontal switches 39' jointly make up a second signal holding circuit 52 for holding signals of the pixel MOS transistors after the pixels are reset."

Consequently, it is a strained interpretation to combine elements 38 and 38' to form a single holding circuit when the Yonemoto reference itself clearly teaches against such an interpretation by describing two separate holding circuits 51, 52, each with the components as described above.

Moreover, Yonemoto et al. fails to teach or suggest, "wherein the first sampling circuit samples a light signal and a reset signal from each photocell in the first column," as claimed. The first signal holding circuit 51 of Yonemoto is for "holding signals of the pixel MOS transistors before the pixels are reset." (col. 7, lines 17-18). The second signal holding circuit 52 of Yonemoto is for "holding signals of the pixel MOS transistors after the pixels

are reset." (col. 7, lines 21-22). Neither of these circuits 51, 52 samples two signals (e.g., a light signal and a reset signal) as claimed.

Furthermore, FIGS. 1 and 4 of Yonemoto et al. clearly show that element 38 is a capacitor that has a first terminal that is coupled to a node, which is coupled to the source electrode of transistor 37 and the drain electrode of transistor 39, and a second terminal that is coupled to a ground potential. Similarly, FIG. 1 and 4 of Yonemoto et al. clearly indicate that element 38' is a capacitor that has a first terminal that is coupled to a node, which is coupled to the source electrode of transistor 37' and the drain electrode of transistor 39', and a second terminal that is coupled to a ground potential. In either case, the second terminal of the capacitor (38 or 38') is coupled to the ground potential and not coupled to the first electrode of the first switch as claimed.

In other words, Yonemoto utilizes a first capacitor 38 for sampling the signal value before pixel reset and a second, separate capacitor 38' for sampling the signal value after pixel reset. Moreover, Yonemoto clearly indicates that two sample and hold circuits (a first signal holding circuit 51 and a second signal holding circuit 52) are utilized per column in its solid-state imaging device. In sharp contrast, the claimed invention employs for each column a single sampling circuit that samples both a light signal and a reset signal from a photocell as claimed.

The dependent claims incorporate all the limitations of independent claim 22, respectively. In this regard, the dependent claims also add additional limitations, thereby making the dependent claims a fortiori and independently patentable over the cited reference.

In view of the foregoing, it is respectfully submitted that Yonemoto reference, whether alone or in combination, fails to teach or suggest the sequential readout circuit and system as claimed.

Claims 15, 16, 17, 23, 24, 26, 29 and 30

Claims 15, 16, 17, 23, 24, 26, 29 and 30 are rejected under 35 U.S.C. 102(e) for the reasons set forth on pages 3-4 of the Action. Specifically, claims 15, 16, 17, 23, 24, 26, 29 and 30 are rejected under 35 U.S.C. 102(e) as being anticipated by Yonemoto et al. (US Pat. No. 6,166,769), which is hereinafter referred to as "Yonemoto" or as "the Yonemoto reference."

The rejections under 35 U.S.C. 102(e) are respectfully traversed, and reconsideration and reexamination of the application is respectfully requested for the reasons set forth herein below.

It is respectfully submitted that the Yonemoto reference fails to teach or suggest each and every element of the circuit as claimed. Specifically, the Yonemoto reference fails to teach or suggest, the first sampling circuit as claimed in claim 23. For example, the Action cites elements 38 and 38' of Yonemoto et al. taken together to teach the first sampling circuit as claimed. However, elements 38 and 38', whether alone, or in combination fail to fairly teach or suggest the first sampling circuit, the first switch, and the specific limitations regarding the coupling between the first sampling circuit and the first switch as required by independent claim 23.

Consequently, it is a strained interpretation to combine elements 38 and 38' to form a single holding circuit when the Yonemoto reference itself clearly teaches against such an interpretation by describing two separate holding circuits 51, 52, each with the components as described above.

Moreover, Yonemoto et al. fails to teach or suggest, "wherein the first sampling circuit samples a light signal and a reset signal from each photocell in the first column," as

recited by claim 23. The first signal holding circuit 51 of Yonemoto is for "holding signals of the pixel MOS transistors before the pixels are reset." (col. 7, lines 17-18). The second signal holding circuit 52 of Yonemoto is for "holding signals of the pixel MOS transistors after the pixels are reset." (col. 7, lines 21-22). Neither of these circuits 51, 52 samples two signals (e.g., a light signal and a reset signal) as claimed.

As advanced previously, FIGS. 1 and 4 of Yonemoto et al. clearly show that element 38 is a capacitor that has a first terminal that is coupled to a node, which is coupled to the source electrode of transistor 37 and the drain electrode of transistor 39, and a second terminal that is coupled to a ground potential. Similarly, FIG. 1 and 4 of Yonemoto et al. clearly indicate that element 38' is a capacitor that has a first terminal that is coupled to a node, which is coupled to the source electrode of transistor 37' and the drain electrode of transistor 39', and a second terminal that is coupled to a ground potential. In either case, the second terminal of the capacitor (38 or 38') is coupled to the ground potential and not coupled to the first electrode of the first switch as claimed.

In other words, Yonemoto utilizes a first capacitor 38 for sampling the signal value before pixel reset and a second, separate capacitor 38' for sampling the signal value after pixel reset. Moreover, Yonemoto clearly indicates that two sample and hold circuits (a first signal holding circuit 51 and a second signal holding circuit 52) are utilized per column in its solid-state imaging device. In sharp contrast, the claimed invention employs for each column a single sampling circuit that samples both a light signal and a reset signal from a photocell as claimed.

The dependent claims incorporate all the limitations of independent claim 23, respectively. In this regard, the dependent claims also add additional limitations, thereby making the dependent claims a fortiori and independently patentable over the cited reference.

In view of the foregoing, it is respectfully submitted that Yonemoto reference, whether alone or in combination, fails to teach or suggest the sequential readout circuit and system as claimed.

Rejection under 35 U.S.C. 103(a) over Yonemoto et al. (U.S. Pat. No. 6,166,769) in view of Simerly et al. (U.S. Pat. No. 5,982,424)

Claims 6, 7, 15 and 16

THE PROPOSED COMBINATION IS BASED ON IMPERMISSIBLE USE OF THE CLAIMED INVENTION AS A TEMPLATE TO PIECE TOGETHER THE TEACHINGS OF THE YONEMOTO REFERENCE AND THE SIMERLY REFERENCE

It is respectfully submitted that the Yonemoto and Simerly references are improperly combined. It appears that the Action uses improper hindsight gained from the claimed invention to select certain components from Yonemoto and other components from Simerly to arrive at the claimed invention.

First, it is respectfully submitted that the Kitagawa reference does not explicitly or implicitly teach or suggest any motivation to combine the Kitagawa reference with the Kamo reference or any motivation to modify the Kitagawa single lens design with a selected diffractive surface from the Kamo reference. Furthermore, it is respectfully submitted that the Kamo reference does not explicitly or implicitly teach or suggest any motivation to employ a diffractive surface for the purpose of color correction in a single lens design.

The Action suggests combining the "dynamic range manipulation" (i.e., adjusting the contrast "to account for variations between frames in the distribution of pixel values") as set forth in col. 7, lines 35-47 of Simerly into the device of Yonemoto.

However, it is respectfully submitted that neither the Yonemoto reference nor the Simerly reference explicitly or implicitly teaches or suggests any motivation to add any

circuits across the negative input terminal and the output terminal of the amplifier 43 (see FIG. 4) for level shifting or gain manipulation as claimed. For example, FIG. 4 only shows the typical feedback capacitor (e.g., 44) and a reset switch (e.g., M45) coupled across the negative input terminal and the output terminal of the amplifier (see col. 7, lines 44 to 53)

Moreover, it is unclear whether such modification proposed by the Action is enabled by the disclosure of the cited references or whether such a modification or combination is even possible since, as advanced hereinafter, the application to which Simerly is directed is different from the application to which Yonemoto is directed.

Also, it appears that elements 32 and 34 of Simerly et al. are for signal processing of a video signal downstream from the readout circuit as claimed. For example, FIG. 3 of Simerly et al. and related description (col. 5, lines 9-24) clarify that CCD imager IC 24 (in CCD card 20) generates an output signal representing the pixel values. Even level shifter 26 and amplifier 28 of FIG. 3 appear to be downstream from the initial generation of an output signal that represents the pixel value, which is performed by the readout circuit as claimed.

Moreover, the AGC 32 and level shifter 34 of Simerly et al. appear to be utilized for a completely different purpose and application (e.g., image compression and a video telephone application) than the readout circuit as claimed. Specifically, AGC 32 and level shifter 34 appear to be components used by the adaptive compression control mechanism of Simerly et al. to control "the timing of clock pulses (C8) to be compatible with an optimize an MPEG compression engine.") (See col. 5, lines 5-8). Consequently, it is respectfully submitted that AGC 32 and level shifter 34 are very different from and do not fairly teach the gain manipulation and level shifting circuits as claimed.

Assuming arguendo that the CDS 30, level shifter 34, and ASIC 40 of Simerly can be incorporated into the solid state imaging device of Yonemoto, the Federal Circuit has stated,

"The mere fact that the prior art may be modified in the manner suggested by the Examiner does not make the modification obvious unless the prior art suggested the desirability of the modification." In re Fritch, 972 F.2d 1260, 23 USPQ 2d 1780, 1783–84 (Fed. Cir. 1992) [emphasis added].

The Federal Circuit has further held In re Fritch, 972 F.2d 1260, 23 USPQ 2d 1780, 1783 (Fed. Cir. 1992):

> In proceedings before the Patent and Trademark Office, the Examiner bears the burden of establishing a prima facie case of obviousness based upon the prior art. ... "[The Examiner] can satisfy this burden only by showing some objective teaching in the prior art ... would lead that individual to combine the relevant teachings of the references. In re Fine, 837 F.2d 1071, 1074, 5 USPQ 2d 1596, 1598 (Fed. Cir. 1988). [emphasis added.]

Consequently, it appears that the current patent application has been improperly used as a basis for the motivation to combine or modify the components selected from Yonemoto and Simerly to arrive at the claimed invention. Stated differently, the proposed combination of the cited references appear to be based on hindsight since the cited references do not teach or suggest a motivation to combine the respective elements of each reference in the manner proposed by the Action.

The Federal Circuit has held, "It is impermissible to use the claimed invention as an instruction manual or "template" to piece together the teachings of the prior art so that the claimed invention is rendered obvious. This court has previously stated, "[o]ne cannot use hindsight reconstruction to pick and choose among isolated disclosures in the prior art to deprecate the claimed invention." (quoting In re Fine, 837 F.2d 1071, 1075, 5 USPQ 2d 1596, 1600 (Fed. Cir. 1988)), In re Fritch, 23 USPQ 2d 1780, 1784 (Fed. Cir. 1992). [emphasis added.]

Furthermore, the Federal Circuit has held, "The combination of elements from non-analogous sources, in a manner that reconstructs the applicant's invention only with the

benefit of hindsight, is insufficient to present a prima facie case of obviousness. There must be some reason, suggestion, or motivation found in the prior art whereby a person of ordinary skill in the field of the invention would make the combination. That knowledge can not come from the applicant's invention itself." In re Oetiker, 977 F.2d 1443, 24 USPQ 2d 1443, 1446 (Fed. Cir. 1992)

Accordingly, hindsight reconstruction may not be used to pick a component from Yonemoto and another component from Simerly to arrive at the invention as claimed. Accordingly, it is respectfully requested that the rejection of claims 6, 7, 15 and 16 under 35 U.S.C. 103(a) be withdrawn.

In view of the foregoing, it is respectfully submitted that the Yonemoto reference, whether alone or in combination with the Simerly reference, fails to teach or suggest the system and circuit as claimed. Accordingly, it is respectfully requested that the claim rejections under 35 U.S.C. Section 103(a) be withdrawn.

EVEN IF PROPERLY COMBINED, THE YONEMOTO REFERENCE AND THE SIMERLY REFERENCE FAIL TO TEACH OR SUGGEST THE SPECIFIC LIMITATIONS SET FORTH BY THE INDEPENDENT AND DEPENDENT CLAIMS

It is respectfully submitted that even if the Yonemoto and Simerly references were properly combined, which is not conceded, the Yonemoto and Simerly references would still fail to teach or suggest specific limitation recited by the claims. It is noted that the dependent claims 6, 7, 15 and 16 incorporate all the limitations of independent claims 22 and 23, respectively. Furthermore, the dependent claims also add additional limitations, thereby making the dependent claims a fortiori and independently patentable over the cited references.

These claims are patentable over the references (when considered either singly or in proposed combination) in view of the shortcomings of Yonemoto as discussed above.

Furthermore, Simerly fails to cure the deficiencies in teaching of Yonemoto. For example, Yonemoto et al., whether alone or in combination with Simerly, fails to teach or suggest, "wherein the first sampling circuit samples a light signal and a reset signal from each photocell in the first column," as recited by claims 22 and 23.

In view of the foregoing, it is respectfully submitted that the Yonemoto reference, whether alone or in combination with the Simerly reference, fails to teach or suggest the single lens as claimed. Accordingly, it is respectfully requested that the claim rejections under 35 U.S.C. Section 103(a) be withdrawn.

Rejection under 35 U.S.C. 103(a) over Yonemoto et al. (U.S. Pat. No. 6,166,769) in view of Krymski et al. (U.S. Pat. No. 6,222,175)

Claims 8 and 17

These claims are patentable over the references (when considered either singly or in proposed combination) in view of the shortcomings of Yonemoto as discussed above. Furthermore, Krymski fails to cure the deficiencies in teaching of Yonemoto. For example, Yonemoto et al., whether alone or in combination with Krymski, fails to teach or suggest, "wherein the first sampling circuit samples a light signal and a reset signal from each photocell in the first column," as recited by claims 22 and 23.

In view of the foregoing, it is respectfully submitted that the Yonemoto reference, whether alone or in combination with the Krymski reference, fails to teach or suggest the single lens as claimed. Accordingly, it is respectfully requested that the claim rejections under 35 U.S.C. Section 103(a) be withdrawn.

CONCLUSION

For the reasons advanced above, Appellant respectfully contends that each claim is patentable. Therefore, reversal of all rejections is courteously solicited.

Respectfully submitted.

Eric Ho

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Date: July 19, 2006
I hereby certify that this paper is being facsimile transmitted to the U.S. Patent and Trademark Office (fax no.: 571-273-8300) on the date below.

Eric Ho

Eric Ho — July 19, 2006 (Date)

viii) CLAIMS APPENDIX

Claim 3 (previously presented): The system of claim 22

wherein each photocell generates a light signal and a reset signal;

wherein the sequential readout circuit determines a difference between the light signal and the reset signal for each photocell in the array in a time sequential manner.

Claim 5 (previously presented): The system of claim 22 further comprising:

an integration capacitor having a first electrode for coupling to the input of the amplifier and a second electrode for coupling to the output of the amplifier; wherein the amplifier includes a charge transfer mode and a unity gain mode.

Claim 6 (previously presented): The system of claim 22 wherein the sequential readout circuit includes

a level shifting circuit that includes a first electrode coupled to the negative input terminal of the amplifier and a second electrode coupled to the output terminal of the amplifier for performing level shifting of the output of the amplifier.

Claim 7 (previously presented): The system of claim 22 wherein the sequential readout circuit includes

a gain manipulation circuit that includes a first electrode coupled to the negative input terminal of the amplifier and a second electrode coupled to the output terminal of the amplifier for performing gain manipulation of the amplifier.

Claim 8 (previously presented): The system of claim 22 wherein each photocell includes

a photodiode for detecting light and responsive thereto for generating a voltage representation thereof; wherein the photodiode includes an integration node;

a gain mechanism that includes a first electrode coupled to the negative input terminal of the amplifier and a second electrode coupled to the output terminal of the amplifier for performing gain manipulation of the amplifier.

Claim 17 (previously presented): The sequential readout circuit of claim 23 wherein each photocell includes

a photodiode for detecting light and responsive thereto for generating a voltage representation thereof: wherein the photodiode includes an integration node;

a first transistor coupled to the photodiode for resetting the integration node in response to a reset signal;

a second transistor coupled to the integration node for shifting the level of the voltage at the integration node: and

a third transistor coupled to the second transistor for reading out the level-shifted voltage in response to a read signal.

Claim 22 (previously presented): A system comprising:

a) an array of photocells that are arranged in rows and columns; and

b) a sequential readout circuit for sequentially reading out the value of the photocells one photocell at a time; wherein the sequential readout circuit includes:

a first sampling circuit that includes a first electrode for coupling to a first column and a second electrode:

a first switch that includes a first electrode coupled to the second electrode of the first sampling circuit, a second electrode, and a third electrode for receiving a first sample control signal; wherein the first switch selectively couples the first electrode of the first switch to the second electrode of the first switch when the first sample control signal is asserted; wherein the first sampling circuit samples a light signal and a reset signal from each photocell in the first column;

a second sampling circuit that includes a first electrode for coupling to a second column and a second electrode;

a second switch that includes a first electrode coupled to the second electrode of the second sampling circuit, a second electrode, and a third electrode for receiving a second sample control signal; wherein the second switch selectively couples the first electrode of the second switch to the second electrode of the second switch when the second sample control signal is asserted; wherein the second sampling circuit samples a light signal and a reset signal from each photocell in the second column; and

an amplifier that includes a negative input terminal coupled to the second electrode of the first switch and the second electrode of the second switch; wherein the amplifier includes an output terminal for generating a signal that corresponds to the amount of light received by a particular photocell in the array.

Claim 23 (previously presented): A sequential readout circuit for coupling to an array of photocells that includes a plurality of photocells that are arranged in rows and columns, each photocell generating a light signal during a first period of time that represents received light and a reset signal after being reset, the sequential readout circuit comprising:

a first sampling circuit that includes a first electrode for coupling to a first column and a second electrode;

a first switch that includes a first electrode coupled to the second electrode of the first sampling circuit, a second electrode, and a third electrode for receiving a first sample control signal; wherein the first switch selectively couples the first electrode of the first switch to the second electrode of the first switch when the first sample control signal is asserted; wherein the first sampling circuit samples a light signal and a reset signal from each photocell in the first column;

a second sampling circuit that includes a first electrode for coupling to a second column and a second electrode;

a second switch that includes a first electrode coupled to the second electrode of the second sampling circuit, a second electrode, and a third electrode for receiving a second sample control signal; wherein the second switch selectively couples the first electrode of the second switch to the second electrode of the second switch when the second sample control signal is asserted; wherein the second sampling circuit samples a light signal and a reset signal from each photocell in the second column;

an amplifier that includes a negative input terminal coupled to the second electrode of the first switch and second electrode of the second switch; wherein the amplifier includes an output terminal for generating a signal that corresponds to the amount of light received by a particular photocell in the array.

Claim 24 (previously presented): The sequential readout circuit of claim 23 wherein the sequential readout circuit sequentially reads out a value of the photocells one photocell at a time

Claim 25 (previously presented): The system of claim 22 wherein the sequential readout circuit measures a light signal from a photocell, measures a reset signal from a photocell, and stores a charge that represents the difference between the light signal and the reset signal.

Claim 26 (previously presented): The sequential readout circuit of claim 23 wherein the sequential readout circuit measures the light signal from a photocell, measures the reset signal from a photocell, and stores a charge that represents the difference between the light signal and the reset signal.

Claim 27 (previously presented): The system of claim 22 wherein the first sampling circuit includes a sampling capacitor.

Claim 28 (previously presented): The system of claim 22 wherein the second sampling circuit includes a sampling capacitor.

Claim 29 (previously presented): The sequential readout circuit of claim 23 wherein the first sampling circuit includes a sampling capacitor.

Claim 30 (previously presented): The sequential readout circuit of claim 23 wherein the second sampling circuit includes a sampling capacitor.

ix) EVIDENCE APPENDIX: none

x) RELATED PROCEEDINGS APPENDIX: none

a first transistor coupled to the photodiode for resetting the integration node in response to a reset signal;

a second transistor coupled to the integration node for shifting the level of the voltage at the integration node; and

a third transistor coupled to the second transistor for reading out the level-shifted voltage in response to a read signal.

Claim 11 (previously presented): The sequential readout circuit of claim 23 wherein the amplifier determines the difference between the light signal and the reset signal for the photocells in the array in a time sequential manner.

Claim 14 (previously presented): The sequential readout circuit of claim 23 wherein the amplifier includes a charge transfer mode, a unity gain mode, a first input; and an output; and

wherein the circuit further includes an integration capacitor having a first electrode for coupling to the negative input terminal and a second electrode for coupling to the output terminal of the amplifier.

Claim 15 (previously presented): The sequential readout circuit of claim 23 further comprising:

a level-shifting mechanism that includes a first electrode coupled to the negative input terminal of the amplifier and a second electrode coupled to the output terminal of the amplifier for performing level shifting of the output of the amplifier.

Claim 16 (previously presented): The sequential readout circuit of claim 23 further comprising: